(14) Please add new claim 17 as follows:

17. (New) The method of claim 16 in which the additional offset combined with any internal offset of the chopper stabilized circuit has a value greater than expected in normal use with a chopper stabilized circuit.

REMARKS

Claims 1-12 are pending in the Application.

Claims 1-9, 11 and 12 stand rejected.

Claim 10 has been cancelled hereinabove.

New claims 13, 14, 15, 16 and 17 have been added.

I. REJECTION UNDER 35 U.S.C. §112, SECOND PARAGRAPH

Claims 1 and 5 have been rejected under 35 U.S.C. §112, second paragraph as failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Claims 1 and 5 have been rejected on the ground that the phrase "one may infer" as a relative term, which renders the claims indefinite. Claims 1 and 5 have been amended hereinabove to delete the clause "whereby one may infer that 1/f noise is within specification," in its entirety. Accordingly, the Applicant respectfully asserts that claims 1 and 5 as rewritten are allowable under 35 U.S.C. § 112, second paragraph, and respectfully requests the Examiner to withdraw the rejection of claims 1 and 5 under 35 U.S.C. §112, second paragraph.

II. REJECTION UNDER 35 U.S.C. §102

Claims 1-9 and 12 have been rejected under 35 U.S.C. §102 as being anticipated by *Lewicki*, U.S. Patent No. 6,351,506 (the "*Lewicki*" reference). The Applicant respectfully traverses the rejections of claims 1-9 and 12 under 35 U.S.C. §102.

Claim 1, as rewritten hereinabove, is directed to an apparatus for testing an integrated circuit to determine if 1/f noise of a circuit to be tested on the integrated circuit is within specifications. The apparatus includes a mechanism for applying a preselected offset inside a chopper stabilized circuit forming part of the circuit to be tested and a circuit for checking whether the output of the chopper stabilized circuit is within a predetermined offset specification for the chopper stabilized circuit. The Examiner contends that the *Lewicki* reference teaches a method and apparatus for testing an integrated circuit comprising a mechanism for applying an offset inside a chopper stabilized circuit forming part of the circuit and a circuit for checking whether the output of the chopper is within specification using a 1/f noise specification. (Paper No. 5, page 3.)

The teaching directed to applying an offset inside the chopper stabilized circuit is explained in *Lewicki* as an offset compensation technique for high gain switched capacitor filters in which chopper stabilization is used in the amplifier within the filter to reduce offsets. (*Lewicki*, column 2, lines 48-54.) The signal at the chopper signal frequency is filtered out with a switched capacitor filter having a cosine filter response in which the combination of chopper stabilization and switch capacitor cosine filtering virtually eliminates offsets without creating extraneous frequency components in the output of the high gain filter circuit. (*Lewicki*, column 2, lines 54-60.) Thus, the referred teaching in the *Lewicki* reference does not disclose a mechanism for applying an offset inside a chopper stabilized circuit. On the contrary, the *Lewicki* reference discloses a technique for compensating offset which would be recognized by those of ordinary skill in the art to rely on well established principles and sampling theory that the DC residual offset in the amplifier is shifted to the chopper signal frequency as a consequence of the sampling represented by the chopper stabilization. The switched capacitor filter then filters out the tone at the chopping frequency, the amplitude of which corresponds to the residual DC offset in the amplifier. Consequently, the Applicant respectfully contends that the *Lewicki* reference does not teach a mechanism for applying an offset inside a chopper stabilized circuit and thus, necessarily, does not teach applying a preselected offset inside a chopper stabilized circuit.

With respect to the limitation drawn to a circuit for checking whether the output of the chopper stabilized circuit is within an offset specification, the *Lewicki* reference teaches a chopper stabilized amplified filter circuit providing a low pass filtered signal with an out of band signal frequency component which is at a frequency of one or more chop control signals and represents an offset and 1/f noise of the chopper stabilized amplified filter circuit. (*Lewicki*, column 9, lines 38-46.) Again, *Lewicki* does not teach a circuit for checking whether the offset is within an offset specification for the amplifier. The teaching in the *Lewicki* reference again refers to the well-established principle that the sampled (that is chopped) signal includes a component at the chopping signal frequency corresponding to the DC offset and a spectrum about the chopping frequency corresponding to the 1/f noise translated by the chopping frequency. Thus, for at least the aforesaid reasons, the *Lewicki* reference does not teach the identical invention of claim 1. Therefore, claim 1 is not anticipated by the *Lewicki* reference, and claim 2 is allowable under 35 U.S.C. §102 over the *Lewicki* reference.

Claim 2 depends from claim 1 and is directed to the apparatus thereof in which the preselected offset has a value greater than expected in normal use with the chopper stabilized circuit. Claim 2 has been rejected on the same teaching as claim 1. (Paper No. 5, page 3.) As a discussion with respect to claim 1 shows, the Examiner has identified nothing in the *Lewicki* reference that discloses an offset having a value greater than expected in normal use with the chopper stabilized circuit. This conclusion is to be expected inasmuch as the *Lewicki* reference is directed to mechanisms for compensating residual offset in a high gain amplifier circuit. Because *Lewicki* does not teach the identical invention of claim 2, claim 2 is allowable under 35 U.S.C. §102 over the *Lewicki* Reference. MPEP §2131.

Claim 3 depends from claim 1 and is directed to the apparatus thereof in which the circuit to be tested passes a 1/f noise test if the output of the chopper stabilized circuit is within the predetermined offset specification. The Examiner alleges that the *Lewicki* reference teaches the limitation of claim 3 in disclosing an input data signal combined with an offset compensation signal and a chopper stabilized amplifier filter circuit providing a low pass filtered signal with an out of band frequency component which is at a frequency of a chop control signal and representing an offset and 1/f noise of the chopper stabilized filter circuit and an output filter

circuit providing a filtered output data signal in which the out of band signal frequency component is substantially reduced in magnitude. (*Lewicki*, column 3, lines 1-15.) This disclosure in the *Lewicki* reference includes no teaching with respect to passing a 1/f noise test. The *Lewicki* reference teaches that a residual offset may be reduced by upshifting it to the chopping (that is sampling) frequency and then filtering out that frequency from the output data. The amplifier 1/f noise is similarly upshifted to form a spectral band about the chopping frequency, which may also then be filtered from the output data by the low pass filter. Because the *Lewicki* reference does not teach the identical invention of claim 3, claim 3 is also allowable under 35 U.S.C. §102 over the *Lewicki* reference.

Claim 4 is directed to the apparatus of claim 1 in which the chopper stabilized circuit is a chopper stabilized amplifier. Because claim 4 is a dependent claim, it incorporates the limitations of claim 1 from which it depends by reference. Claim 4 is directed to the apparatus in its entirety, and, for the reasons previously discussed, the *Lewicki* reference necessarily does not teach the invention of claim 4. Consequently, claim 4 is also allowable under 35 U.S.C. §102 over the *Lewicki* reference.

Claim 5 is directed to a method for testing an integrated circuit to determine if 1/f noise of a circuit to be tested on an integrated circuit is within specifications. The method includes applying a preselected offset inside a chopper stabilized circuit forming part of the circuit to be tested and checking whether the output of the chopper stabilized circuit is within a predetermined offset for the chopper stabilized circuit. Claim 5 has been rejected on the identical basis as claim 1. (Paper No. 5, page 3.) For at least the reasons discussed hereinabove in conjunction with claim 1, the Applicant respectfully contends that the *Lewicki* reference also fails to teach the identical invention of claim 5. Consequently, claim 5 is allowable under 35 U.S.C. §102 over the *Lewicki* reference.

Claim 6 depends from claim 5 and recites the method thereof in which the offset has a value greater than expected in normal use with the chopper stabilized circuit. Claim 6 has also been rejected on the identical ground as claims 1 and 2. (Paper No. 5, page 3.) Because, for at least the reasons regarding the teachings of the *Lewicki* reference discussed in conjunction with claim 2, the *Lewicki* reference does not teach the identical invention of claim 6, and the

Applicant also respectfully asserts that claim 6 is also allowable under 35 U.S.C. §102 over the *Lewicki* reference.

Claim 7 is directed to the method of claim 6 in which the circuit to be tested passes a 1/f noise test if the output of the chopper stabilized circuit is within the predetermined offset specification. Claim 7 has been rejected on the same basis as claim 3. (Paper No. 5, page 3.) The Applicant respectfully asserts that claim 7 is also allowable under 35 U.S.C. §102 over the *Lewicki* reference for at least the reasons discussed in conjunction with claim 3.

Claim 8 is directed to the method of claim 5 in which the chopper stabilized circuit is a chopper stabilized amplifier. Similar to claim 4, claim 8 incorporates the limitations of claim 5 from which it depends, and, analogous to claim 4 discussed hereinabove, the *Lewicki* reference does not teach all of the limitations of claim 8. Therefore, the Applicant respectfully contends that claim 8 is allowable under 35 U.S.C. §102 over the *Lewicki* reference.

Claim 9 is directed to a method for testing for 1/f noise performance in less than 1/f time comprising the step of using proper offset removal of a chopper stabilized circuit as a surrogate for measuring for 1/f noise. Claim 9 has been rejected on teaching in the *Lewicki* reference directed to a chopper stabilized amplifier filter circuit providing a low pass filtered signal with an out of band frequency signal component at the frequency of a chop control signal, etc., discussed hereinabove in conjunction with claims 3 and 7. (Paper No. 5, page 3) (citing *Lewicki*, column 3, lines 3-10). The Applicant asserts that nothing in this teaching exists that discloses using proper offset removal as a surrogate for measuring for 1/f noise. As previously discussed, the *Lewicki* reference is directed to shifting the offset and the 1/f noise spectrum by the chopper frequency and filtering out the resulting signals. Because, for at least this reason, the *Lewicki* reference does not teach the identical invention of claim 9, claim 9 is allowable under 35 U.S.C. §102 over the *Lewicki* reference.

Claim 12 has been rejected on the same basis as claim 9. (Paper No. 5, page 3.) As claim 12 has been rewritten hereinabove to depend from claim 11, the Applicant will discuss claim 12 in conjunction with the rejection of claim 11 (as rewritten), below.

III. REJECTION UNDER 35 U.S.C. § 102

Claims 10 and 11 have been rejected under 35 U.S.C. §102 as being anticipated by *Totani, et al.*, Japanese Patent No. JP405235767A (the "*Totani*" reference). The Applicant respectfully traverses the rejections of claims 10 and 11 under 35 U.S.C. §102.

With respect to claim 10, claim 10 has been cancelled hereinabove and is respectfully withdrawn from the Examiner's consideration.

Claim 11, as rewritten hereinabove, is directed to a method of testing an integrated circuit. The method includes, external to the integrated circuit, observing an output of a chopper stabilized circuit and, external to the integrated circuit, controlling an offset of the chopper stabilized circuit. Claim 11 has been rejected over the teaching in the *Totani* reference directed to a chopper type comparator including an offset correction circuit having plural capacitors (C1-C4), each of which has one electrode commonly connected to the input of an inverter (which is also connected to a terminal of an input capacitor (C0)) and also having remaining electrodes that are respectively coupled to outputs of corresponding NOR gates. (*Totani*, Constitution). Thus, *Totani* does not disclose a method of testing an integrated circuit including, external to the circuit, observing an output of a chopper stabilized circuit, and external to the circuit, controlling the offset of the chopper stabilized circuit. The Applicant also respectively submits, for the reasons previously discussed, that the *Lewicki* reference does not teach the invention of claim 11. Thus, for at least these reasons, the Applicant respectfully asserts that claim 11 is allowable under 35 U.S.C. §102 over either the *Totani* reference or the *Lewicki* reference

Claim 12 has been amended to depend from claim 11 and recites the method thereof including using offset removal as a surrogate for 1/f noise performance. As the discussion in conjunction with claim 11, and claims 1-9 above show, neither *Totani* nor *Lewicki* discloses using offset removal of the chopper stabilized circuit as a surrogate for measuring 1/f noise. Consequently, claim 12 is also allowable under 35 U.S.C. §102 over either the *Totani* reference or the *Lewicki* reference.

IV. NEW CLAIMS

New claim 13 is a dependent claim depending from claim 12. Claim 13 recites the circuit under test passes a 1/f noise test if the output of the chopper stabilized circuit is within a predetermined offset specification. For example, this recitation parallels the recitation in claim 3, and the *Lewicki* reference has been discussed in as applied thereto in conjunction with claim 3.

New independent claim 14 is directed to an apparatus for testing an integrated circuit to determine if said integrated circuit is within specifications. The apparatus includes a mechanism for selectively adding additional offset, while the test is conducted, inside a chopper stabilized circuit forming part of said circuit to be tested, and a circuit for checking whether the output of said chopper stabilized circuit is within a predetermined limit. The Applicant respectfully submits that neither the *Lewicki* reference nor the *Totani* reference, for the reasons previously discussed, teach or suggest the limitations of claim 14.

New claim 15 depends from claim 14 and recites the additional offset combined with any internal offset of the chopper stabilized circuit has a value greater than expected in normal use with a chopper stabilized circuit. For example, this recitation parallels the recitation of claim 2, as it relates to the additional offset combined with any internal offset. The Applicant respectfully submits that neither the *Lewicki* reference nor the *Totani* reference, for the reasons previously discussed, teach or suggest the limitations of claim 15.

New claim 16 is directed to a method for testing an integrated circuit to determine if said integrated circuit is within specifications. The method includes selectively adding additional offset while the test is conducted inside a chopper stabilized circuit forming part of said circuit to be tested and checking whether the output level of said chopper stabilized circuit is within a predetermined limit. Claim 16 is the process that is the analog of the apparatus of claim 14.

New claim 17 directed to the method of claim 16 in which the additional offset combined with any internal offset of the chopper stabilized circuit has a value greater than expected in normal use with a chopper stabilized circuit. The recitation of claim 17 parallels the recitation in apparatus claim 15.

V. CONCLUSION

As a result of the foregoing, Applicant asserts that the remaining Claims in the Application are in condition for allowance and respectfully requests an early allowance of such Claims.

Applicant respectfully requests that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

The Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account Number 23-2426 of WINSTEAD SECHREST & MINICK P.C.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.
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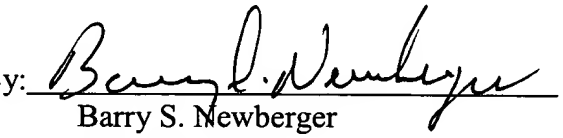
By: 
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VERSION TO SHOW CHANGES

IN THE CLAIMS

(1) Claim 1 has been rewritten as follows:

1. (Amended) An apparatus for testing an integrated circuit to determine if 1/f noise of a circuit to be tested on said integrated circuit is within specifications, comprising:

a. a mechanism for applying a preselected [an] offset inside a chopper stabilized circuit forming part of said circuit to be tested; and

b. a circuit for checking whether the output of said chopper stabilized circuit is within a predetermined offset specification for the chopper stabilized circuit [that is working properly, whereby one may infer that 1/f noise is within specification].

(2) Claim 2 has been rewritten as follows:

2. (Amended) Apparatus of claim 1 in which said preselected offset has a value greater than expected in normal use with the chopper amplifier.

(3) Claim 3 has been rewritten as follows:

3. (Amended) Apparatus of claim 1 in which the circuit to be tested passes a 1/f noise test if the output of the chopper stabilized circuit is within the predetermined offset specification [specifications for a properly working chopper stabilized circuit].

(4) Claim 5 has been rewritten as follows:

5. (Amended) A method for testing an integrated circuit to determine if 1/f noise of a circuit to be tested on said integrated circuit is within specifications, comprising:

a. applying a preselected [an] offset inside a chopper stabilized circuit forming part of said circuit to be tested; and

b. checking whether the output of said chopper stabilized circuit is within a predetermined offset specification for the chopper stabilized circuit [that is working properly, whereby one may infer that 1/f noise is within specification].

(5) Claim 6 has been rewritten as follows:

6. (Amended) Method of claim 5 in which said preselected offset has a value greater than expected in normal use with the chopper amplifier.

(6) Claim 7 has been rewritten as follows:

7. (Amended) Method of claim 5 in which the circuit to be tested passes a 1/f noise test if the output of the chopper stabilized circuit is within the predetermined offset specification [specifications for a properly working chopper stabilized circuit].

(7) Claim 11 has been rewritten as follows:

11. (Amended) A method of [fabricating] testing an integrated circuit comprising [the step of]:

(a) [providing access at the output and control of internal offset] external to the circuit, observing an output of a chopper stabilized circuit; and

(b) external to the circuit, controlling the offset of the chopper stabilized circuit.

(8) Claim 12 has been rewritten as follows:

12. (Amended) [A] The method of [testing an integrated circuit] claim 11 comprising [the steps of controlling the offset at a chopper stabilized circuit and] using offset removal as a surrogate for 1/f noise performance of the chopper stabilized circuit.